FIG. 1

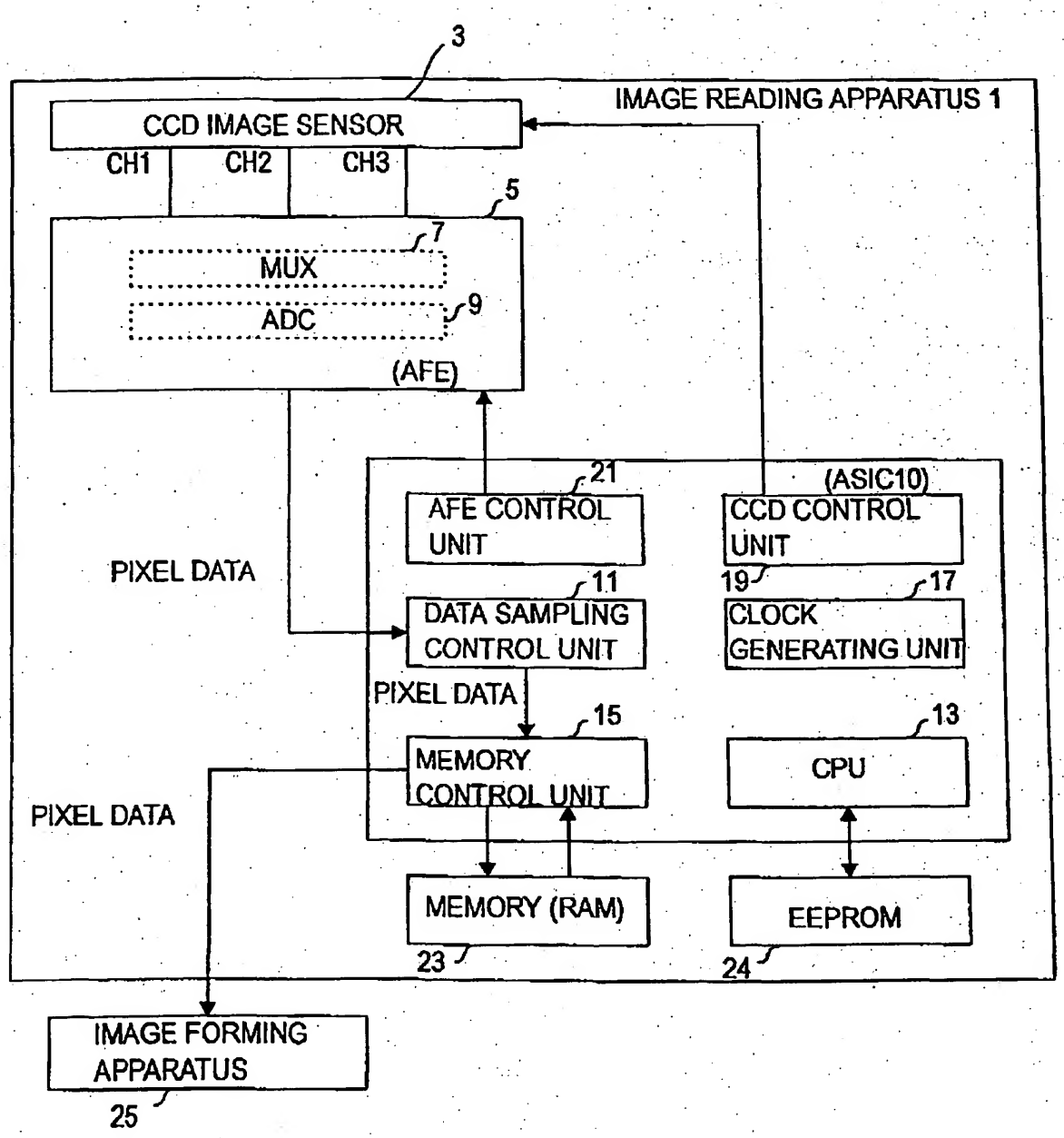

3
IMAGE READING APPARATUS 1
CCD IMAGE SENSOR
CH1
CH2
CH3
5
7
MUX
9
ADC
(AFE)
21
AFE CONTROL UNIT
(ASIC10)
CCD CONTROL UNIT
19
17
CLOCK GENERATING UNIT
PIXEL DATA
11
DATA SAMPLING CONTROL UNIT
PIXEL DATA
15
MEMORY CONTROL UNIT
13
CPU
PIXEL DATA
MEMORY (RAM)
23
EEPROM
24
IMAGE FORMING APPARATUS
25

FIG. 2

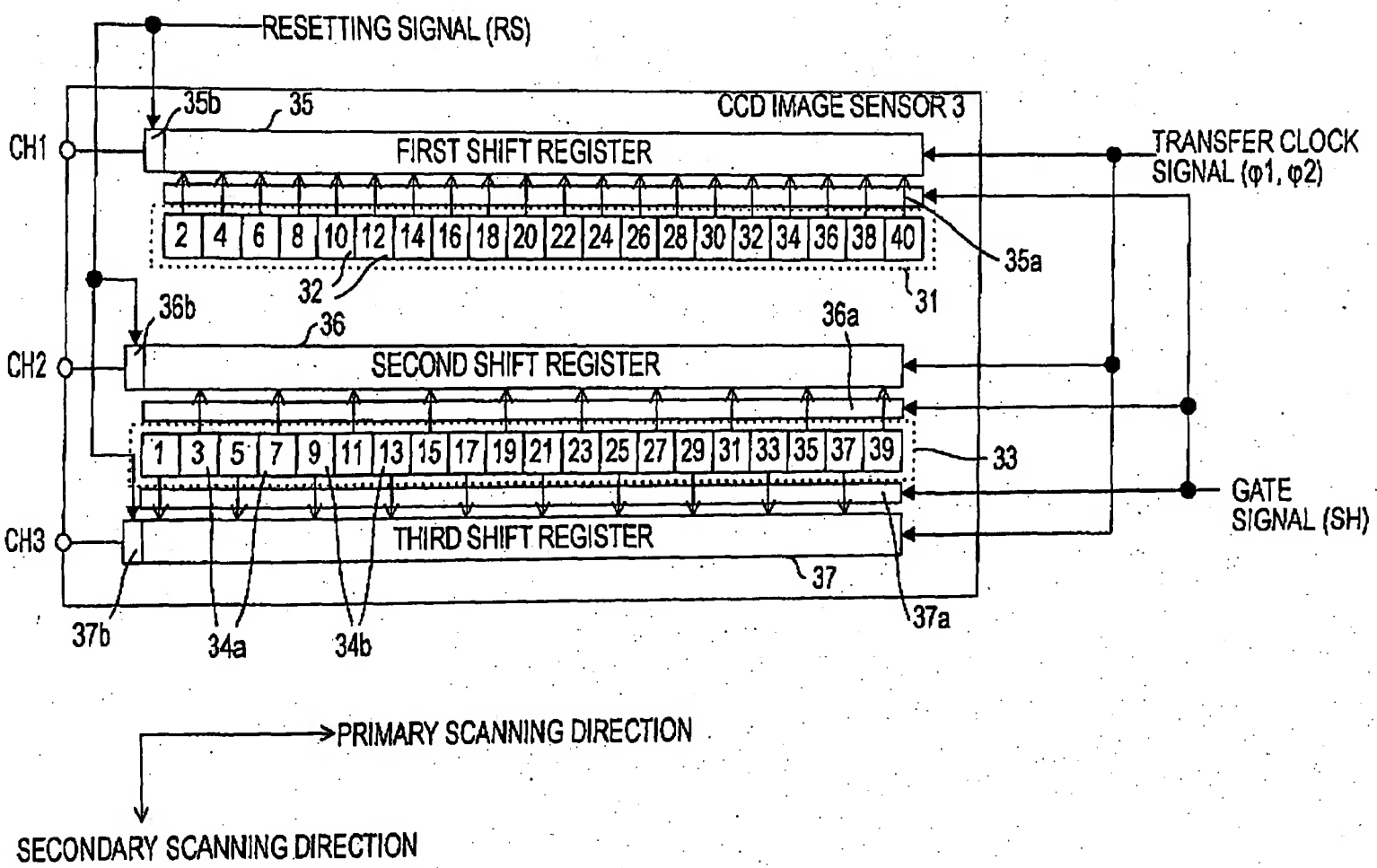

RESETTING SIGNAL (RS)
CCD IMAGE SENSOR 3
35b
35
CH1
FIRST SHIFT REGISTER
TRANSFER CLOCK SIGNAL (φ1, φ2)
2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40
35a
32
31
36b
36
36a
CH2
SECOND SHIFT REGISTER
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39
33
GATE SIGNAL (SH)
CH3
THIRD SHIFT REGISTER
37
37b
34a
34b
37a
PRIMARY SCANNING DIRECTION
SECONDARY SCANNING DIRECTION

FIG. 3

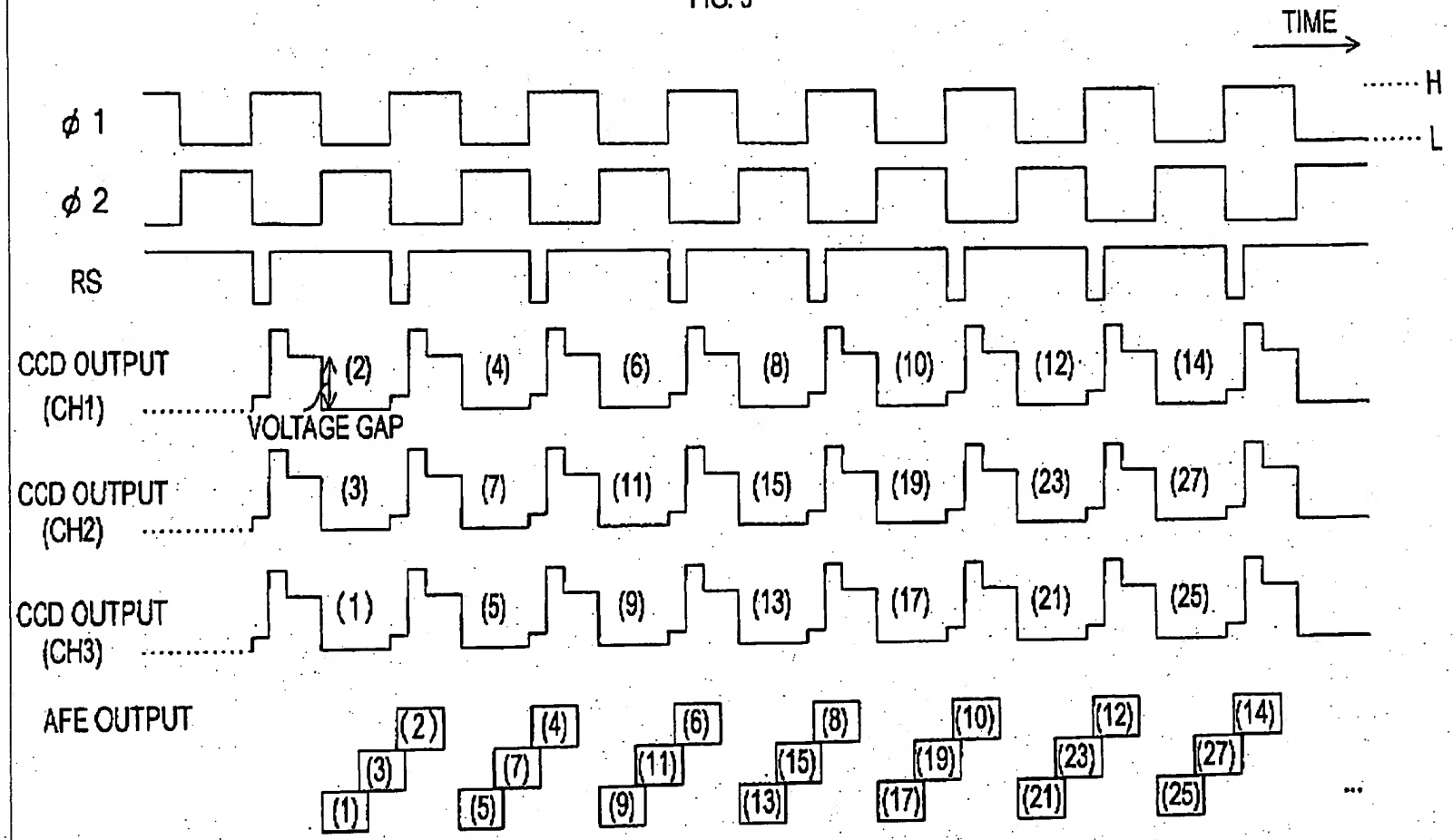

TIME
H
L
ϕ 1
ϕ 2
RS
CCD OUTPUT (CH1)
CCD OUTPUT (CH2)
CCD OUTPUT (CH3)
VOLTAGE GAP
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)
(14)
(15)
(17)
(19)
(21)
(23)
(25)
(27)
AFE OUTPUT

FIG. 4

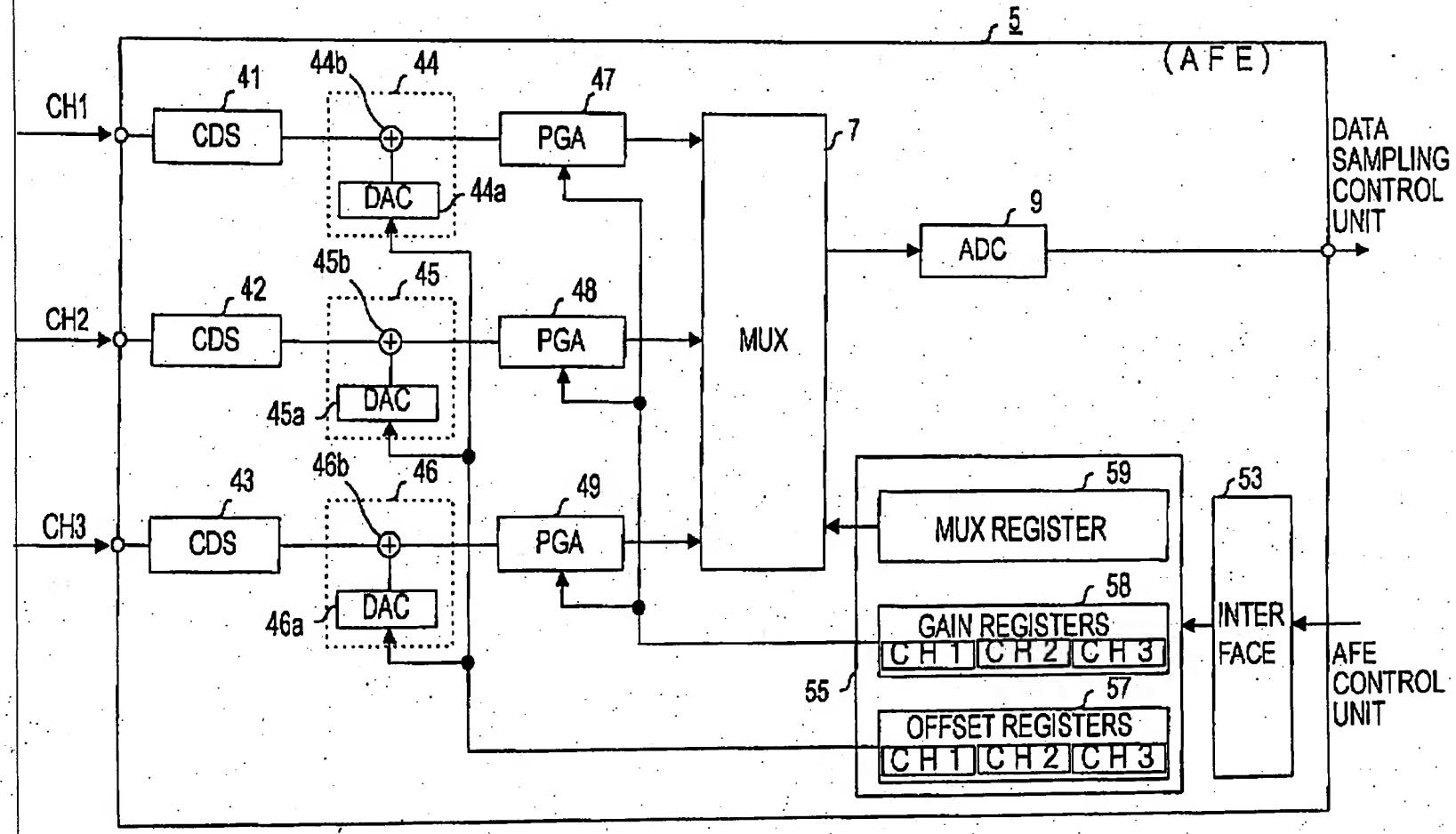

5
(AFE)
CH1
CH2
CH3
41
42
43
CDS
CDS
CDS
44b
44
45b
45
46b
46
DAC
44a
DAC
45a
DAC
46a
47
48
49
PGA
PGA
PGA
7
MUX
9
ADC
DATA SAMPLING CONTROL UNIT
59
MUX REGISTER
58
GAIN REGISTERS
CH1 CH2 CH3
55
57
OFFSET REGISTERS
CH1 CH2 CH3
53
INTER FACE
AFE CONTROL UNIT

FIG. 5

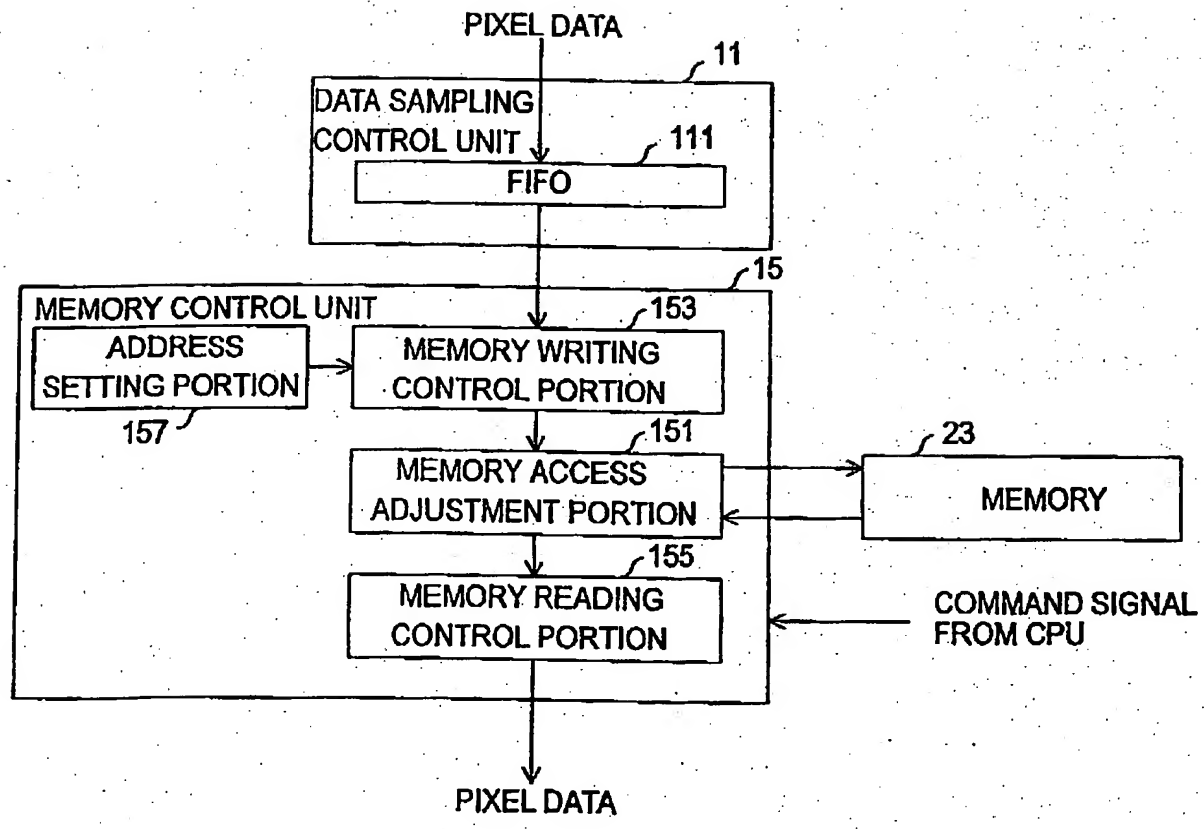

PIXEL DATA
11
DATA SAMPLING CONTROL UNIT
111
FIFO
15
MEMORY CONTROL UNIT
153
ADDRESS SETTING PORTION
MEMORY WRITING CONTROL PORTION
157
151
23
MEMORY ACCESS ADJUSTMENT PORTION
MEMORY
155
MEMORY READING CONTROL PORTION
COMMAND SIGNAL FROM CPU
PIXEL DATA

FIG. 6

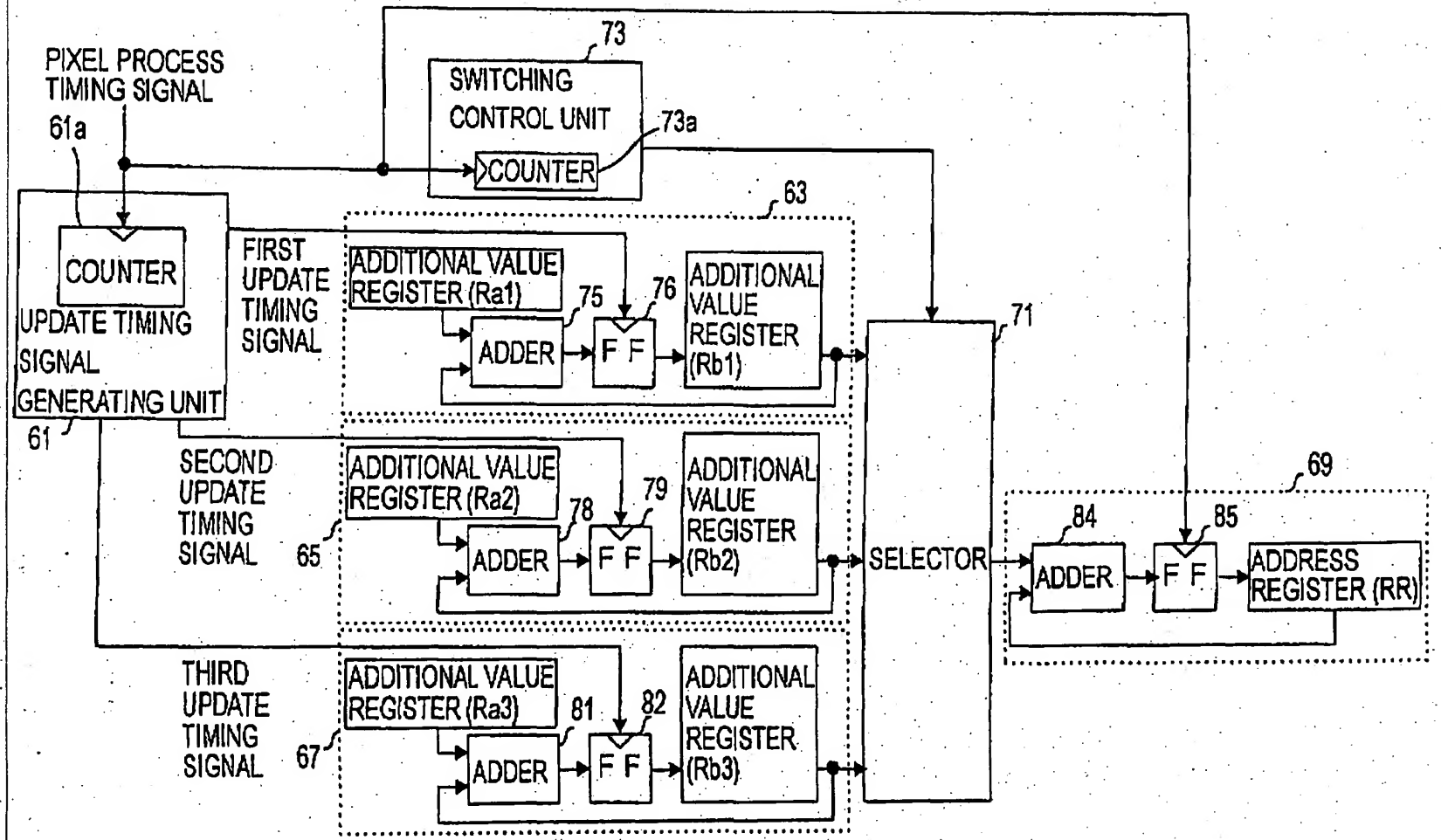

PIXEL PROCESS TIMING SIGNAL
61a
73
SWITCHING CONTROL UNIT
73a
COUNTER
63
COUNTER
UPDATE TIMING SIGNAL GENERATING UNIT
61
FIRST UPDATE TIMING SIGNAL
ADDITIONAL VALUE REGISTER (Ra1)
75
76
ADDER
F F
ADDITIONAL VALUE REGISTER (Rb1)
71
SECOND UPDATE TIMING SIGNAL
65
ADDITIONAL VALUE REGISTER (Ra2)
78
79
ADDER
F F
ADDITIONAL VALUE REGISTER (Rb2)
THIRD UPDATE TIMING SIGNAL
67
ADDITIONAL VALUE REGISTER (Ra3)
81
82
ADDER
F F
ADDITIONAL VALUE REGISTER (Rb3)
SELECTOR
69
84
85
ADDER
F F
ADDRESS REGISTER (RR)

FIG. 7

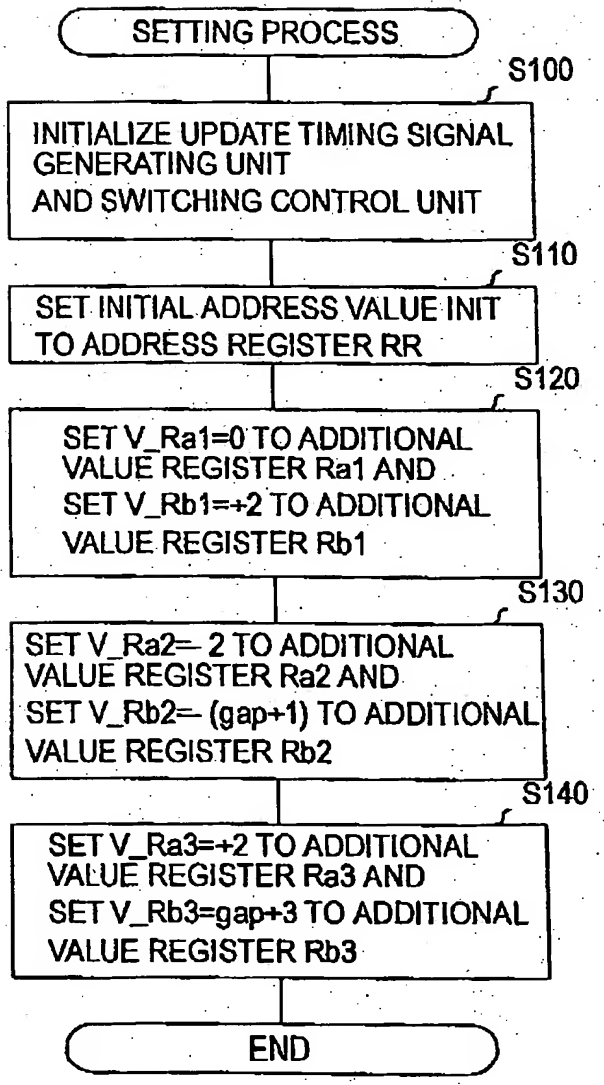

SETTING PROCESS
S100
INITIALIZE UPDATE TIMING SIGNAL GENERATING UNIT AND SWITCHING CONTROL UNIT
S110
SET INITIAL ADDRESS VALUE INIT TO ADDRESS REGISTER RR
S120
SET V_Ra1=0 TO ADDITIONAL VALUE REGISTER Ra1 AND SET V_Rb1=+2 TO ADDITIONAL VALUE REGISTER Rb1
S130
SET V_Ra2=-2 TO ADDITIONAL VALUE REGISTER Ra2 AND SET V_Rb2=-(gap+1) TO ADDITIONAL VALUE REGISTER Rb2
S140
SET V_Ra3=+2 TO ADDITIONAL VALUE REGISTER Ra3 AND SET V_Rb3=gap+3 TO ADDITIONAL VALUE REGISTER Rb3
END

FIG. 8A

OUTPUT ORDER IN PRIMARY SCANNING DIRECTION →

OUTPUT ORDER IN SECONDARY SCANNING DIRECTION ↓

	CH3	CH2	CH1	CH3	CH2	CH1	CH3	CH2	CH1	CH3	CH2	CH1	
	(5,1)	(5,3)	(0,2)	(5,5)	(5,7)	(0,4)	(5,9)	(5,11)	(0,6)	(5,13)	(5,15)	(0,8)	..... → ①
① →	(6,1)	(6,3)	(1,2)	(6,5)	(6,7)	(1,4)	(6,9)	(6,11)	(1,6)	(6,13)	(6,15)	(1,8)	..... → ②
② →	(7,1)	(7,3)	(2,2)	(7,5)	(7,7)	(2,4)	(7,9)	(7,11)	(2,6)	(7,13)	(7,15)	(2,8)	..... → ③
③ →	(8,1)	(8,3)	(3,2)	(8,5)	(8,7)	(3,4)	(8,9)	(8,11)	(3,6)	(8,13)	(8,15)	(3,8)	..... → ④
④ →	(9,1)	(9,3)	(4,2)	(9,5)	(9,7)	(4,4)	(9,9)	(9,11)	(4,6)	(9,13)	(9,15)	(4,8)	..... → ⑤
⑤ →	(10,1)	(10,3)	(5,2)	(10,5)	(10,7)	(5,4)	(10,9)	(10,11)	(5,6)	(10,13)	(10,15)	(5,8)	..... → ⑥
⑥ →	(11,1)	(11,3)	(6,2)	(11,5)	(11,7)	(6,4)	(11,9)	(11,11)	(6,6)	(11,13)	(11,15)	(6,8)	.....

FIG. 8B

LOWER ADDRESS →

HIGHER ADDRESS ↓

	00	01	02	03	04	05	06	07	08	09	0a	0b	
0x05	(5,1)	(5,2)	(5,3)	(5,4)	(5,5)	(5,6)	(5,7)	(5,8)	(5,9)	(5,10)	(5,11)	(5,12)	.....
0x06	(6,1)	(6,2)	(6,3)	(6,4)	(6,5)	(6,6)	(6,7)	(6,8)	(6,9)	(6,10)	(6,11)	(6,12)	.....
0x07	(7,1)		(7,3)		(7,5)		(7,7)		(7,9)		(7,11)		.....
0x08	(8,1)		(8,3)		(8,5)		(8,7)		(8,9)		(8,11)		.....
0x09	(9,1)		(9,3)		(9,5)		(9,7)		(9,9)		(9,11)		.....
0x0a	(10,1)		(10,3)		(10,5)		(10,7)		(10,9)		(10,11)		.....
0x0b	(11,1)		(11,3)		(11,5)		(11,7)		(11,9)		(11,11)		.....

FIG. 9

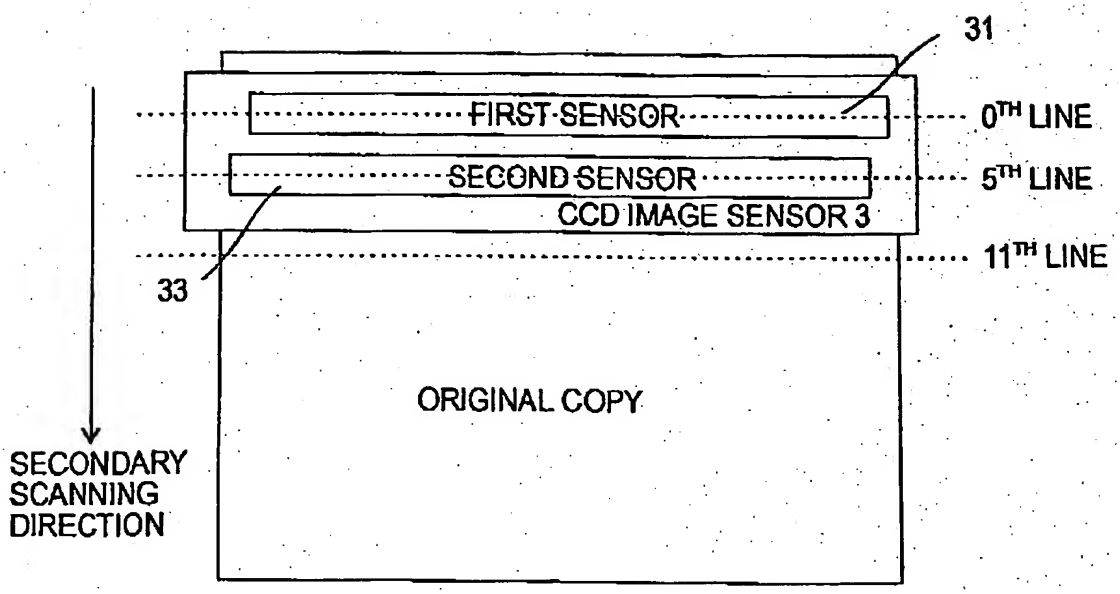

31
FIRST SENSOR
0TH LINE
SECOND SENSOR
5TH LINE
CCD IMAGE SENSOR 3
11TH LINE
33
ORIGINAL COPY
SECONDARY SCANNING DIRECTION

FIG. 10

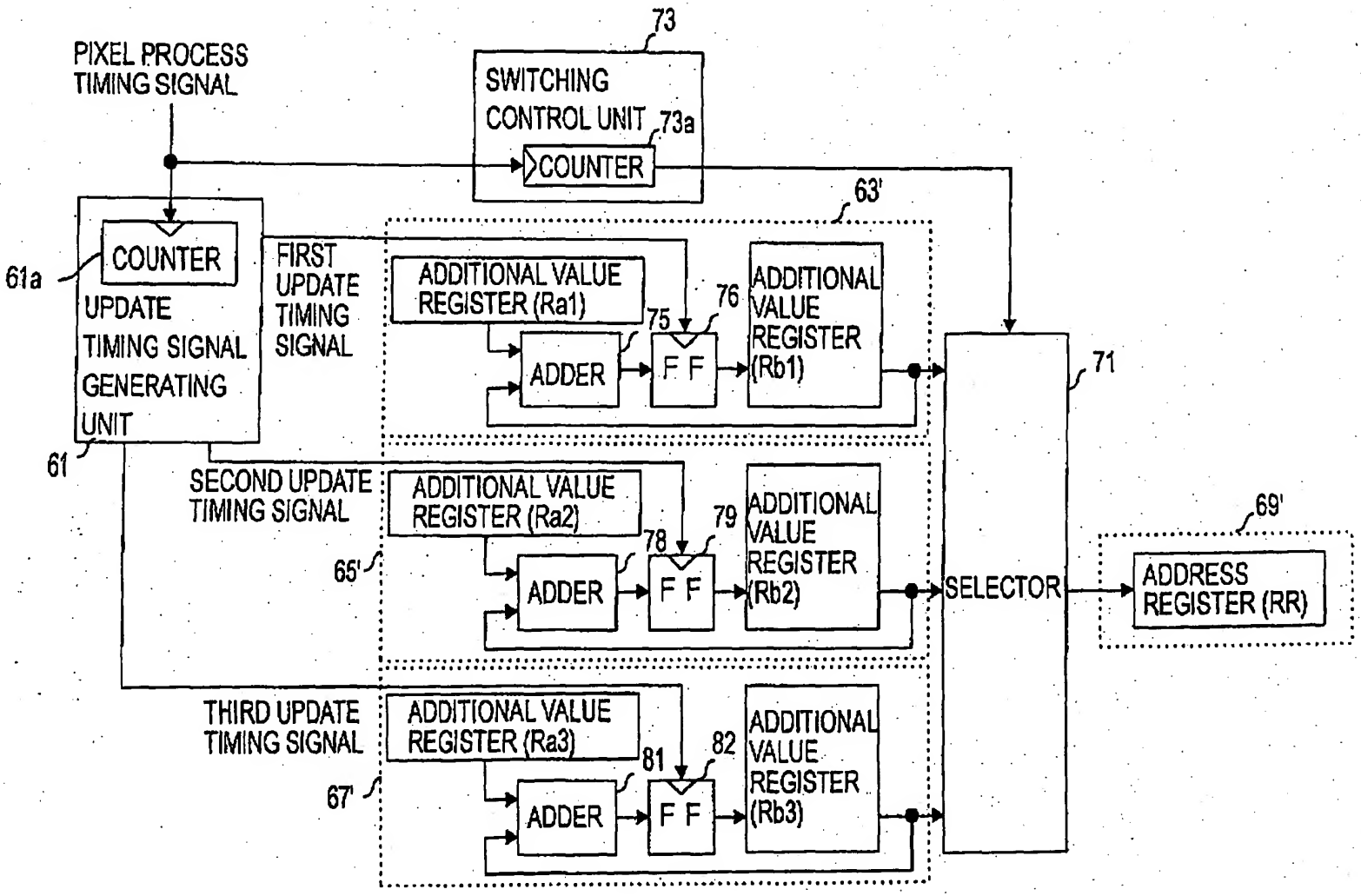

PIXEL PROCESS TIMING SIGNAL
73
SWITCHING CONTROL UNIT
73a
COUNTER
63'
61a
COUNTER
UPDATE TIMING SIGNAL GENERATING UNIT
61
FIRST UPDATE TIMING SIGNAL
ADDITIONAL VALUE REGISTER (Ra1)
75
76
ADDER
F F
ADDITIONAL VALUE REGISTER (Rb1)
71
SECOND UPDATE TIMING SIGNAL
ADDITIONAL VALUE REGISTER (Ra2)
65'
78
79
ADDER
F F
ADDITIONAL VALUE REGISTER (Rb2)
SELECTOR
69'
ADDRESS REGISTER (RR)
THIRD UPDATE TIMING SIGNAL
ADDITIONAL VALUE REGISTER (Ra3)
67'
81
82
ADDER
F F
ADDITIONAL VALUE REGISTER (Rb3)

FIG. 11

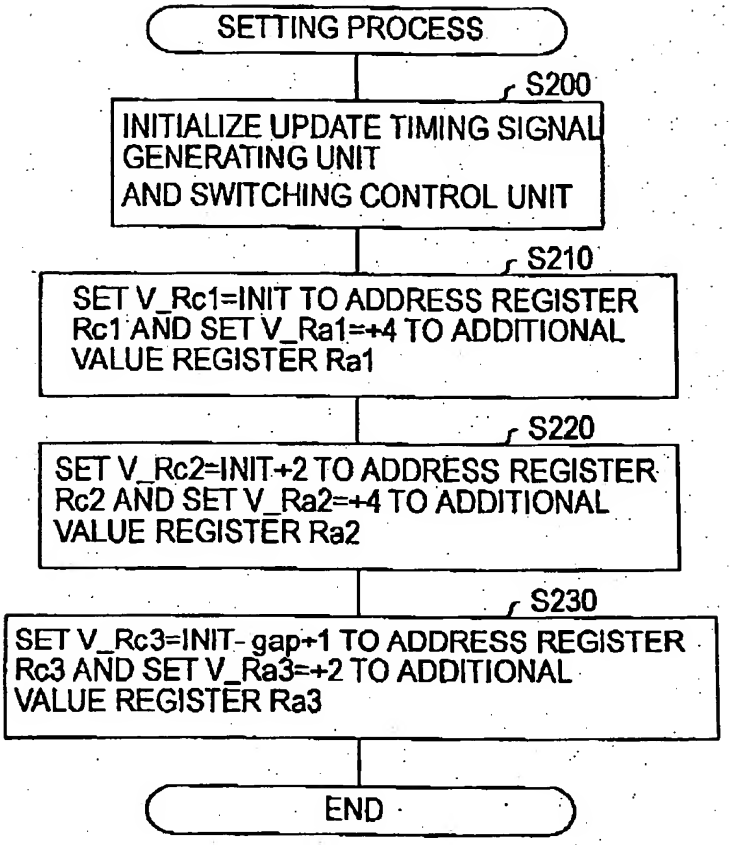

SETTING PROCESS
S200
INITIALIZE UPDATE TIMING SIGNAL GENERATING UNIT AND SWITCHING CONTROL UNIT
S210
SET V_Rc1=INIT TO ADDRESS REGISTER Rc1 AND SET V_Ra1=+4 TO ADDITIONAL VALUE REGISTER Ra1
S220
SET V_Rc2=INIT+2 TO ADDRESS REGISTER Rc2 AND SET V_Ra2=+4 TO ADDITIONAL VALUE REGISTER Ra2
S230
SET V_Rc3=INIT-gap+1 TO ADDRESS REGISTER Rc3 AND SET V_Ra3=+2 TO ADDITIONAL VALUE REGISTER Ra3
END

FIG. 12

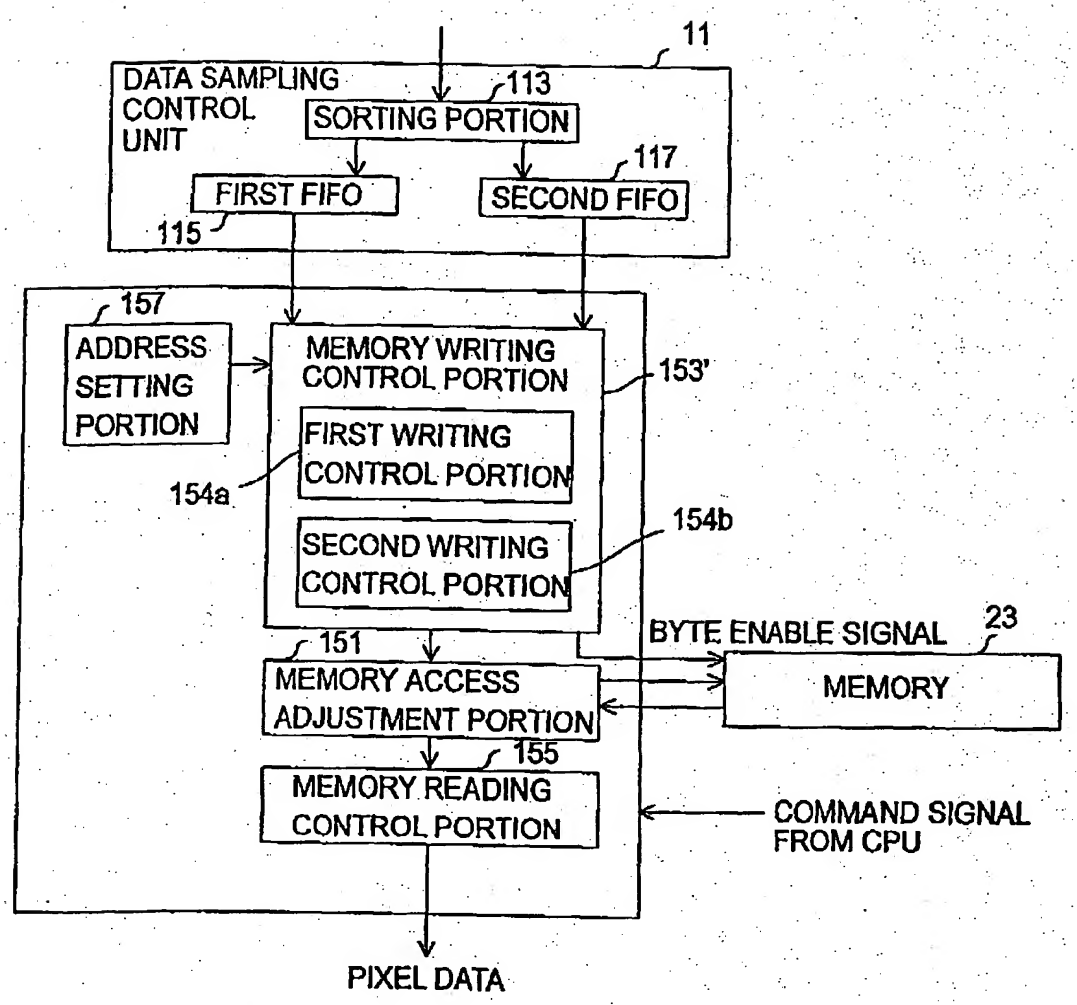

11
DATA SAMPLING CONTROL UNIT
113
SORTING PORTION
117
FIRST FIFO
SECOND FIFO
115
157
ADDRESS SETTING PORTION
MEMORY WRITING CONTROL PORTION
153'
FIRST WRITING CONTROL PORTION
154a
SECOND WRITING CONTROL PORTION
154b
BYTE ENABLE SIGNAL
23
151
MEMORY ACCESS ADJUSTMENT PORTION
MEMORY
155
MEMORY READING CONTROL PORTION
COMMAND SIGNAL FROM CPU
PIXEL DATA

FIG. 13A

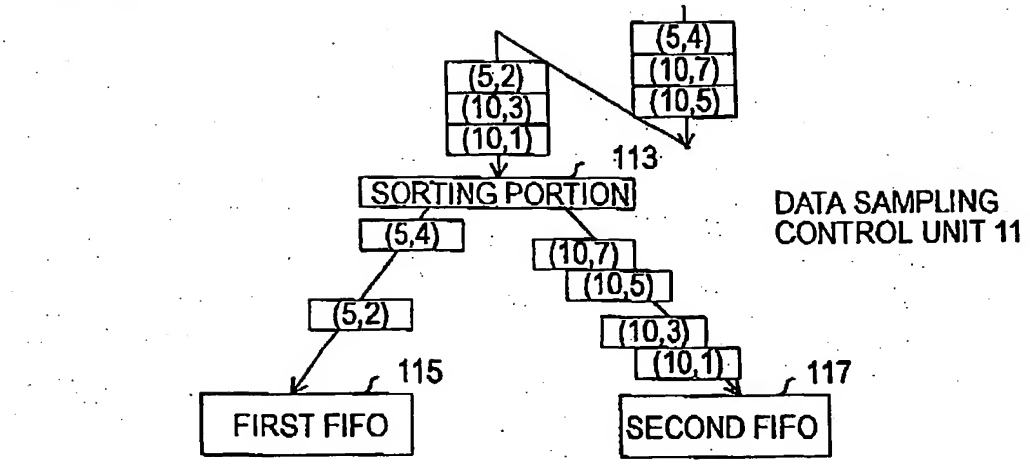


FIG. 13B

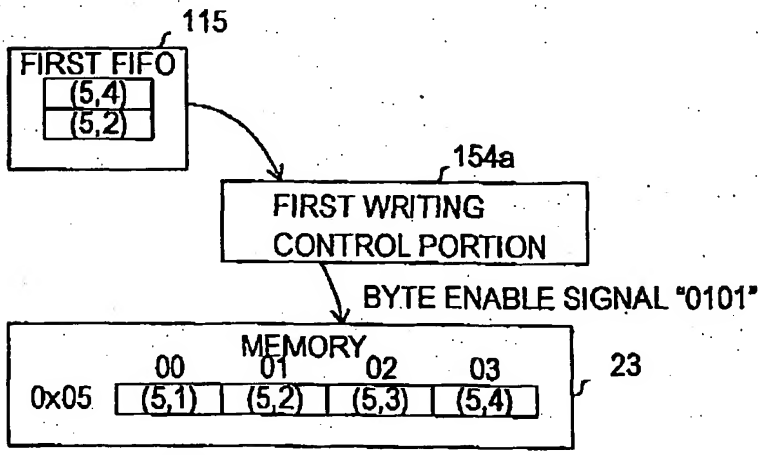


FIG. 13C

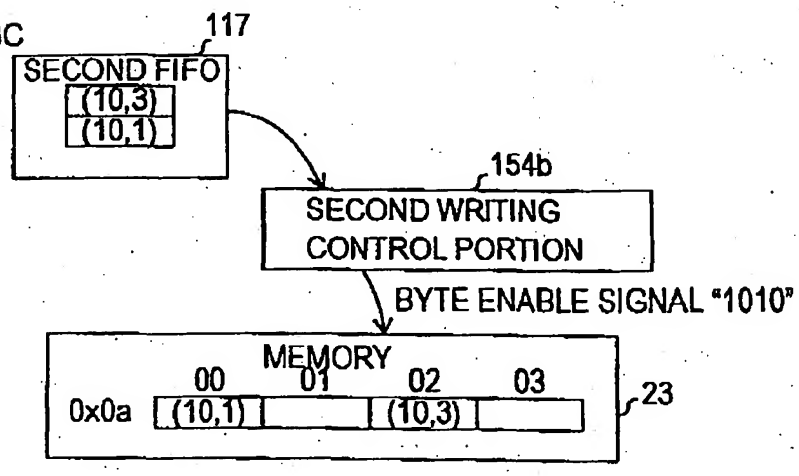


FIG. 14

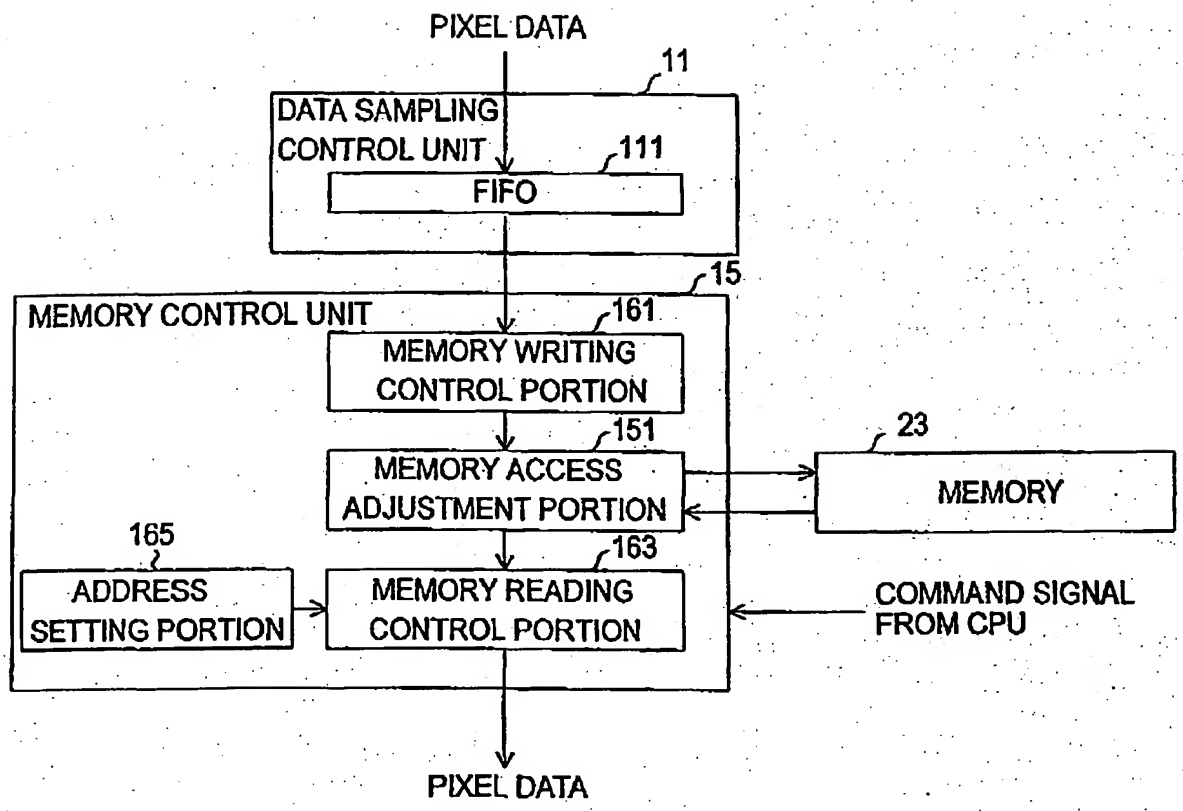

PIXEL DATA
11
DATA SAMPLING CONTROL UNIT
111
FIFO
15
MEMORY CONTROL UNIT
161
MEMORY WRITING CONTROL PORTION
151
MEMORY ACCESS ADJUSTMENT PORTION
23
MEMORY
165
ADDRESS SETTING PORTION
163
MEMORY READING CONTROL PORTION
COMMAND SIGNAL FROM CPU
PIXEL DATA

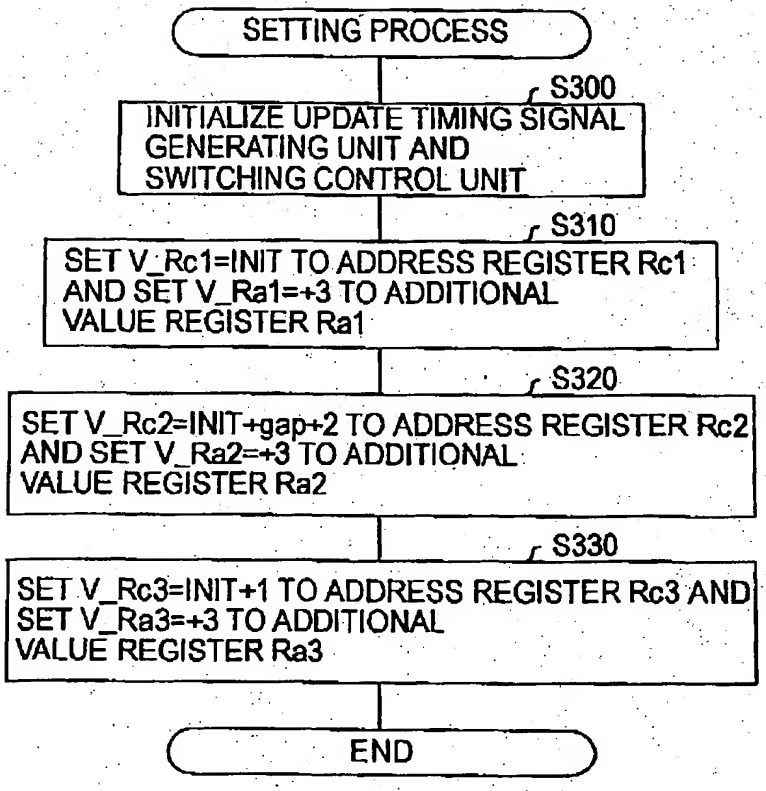
FIG. 15A

HIGHER ADDRESS \ LOWER ADDRESS	00	01	02	03	04	05	06	07	08	09	0a	0b	
0x05	(5,1)	(5,3)	(0,2)	(5,5)	(5,7)	(0,4)	(5,9)	(5,11)	(0,6)	(5,13)	(5,15)	(0,8)	.....
0x06	(6,1)	(6,3)	(1,2)	(6,5)	(6,7)	(1,4)	(6,9)	(6,11)	(1,6)	(6,13)	(6,15)	(1,8)	.....
0x07	(7,1)	(7,3)	(2,2)	(7,5)	(7,7)	(2,4)	(7,9)	(7,11)	(2,6)	(7,13)	(7,15)	(2,8)	.....
0x08	(8,1)	(8,3)	(3,2)	(8,5)	(8,7)	(3,4)	(8,9)	(8,11)	(3,6)	(8,13)	(8,15)	(3,8)	.....
0x09	(9,1)	(9,3)	(4,2)	(9,5)	(9,7)	(4,4)	(9,9)	(9,11)	(4,6)	(9,13)	(9,15)	(4,8)	.....
0x0a	(10,1)	(10,3)	(5,2)	(10,5)	(10,7)	(5,4)	(10,9)	(10,11)	(5,6)	(10,13)	(10,15)	(5,8)	.....
0x0b	(11,1)	(11,3)	(6,2)	(11,5)	(11,7)	(6,4)	(11,9)	(11,11)	(6,6)	(11,13)	(11,15)	(6,8)	.....

FIG. 15B

	HIGHER ADDRESS											
ADDRESS REGISTER Rc1	0x05-	00			03			06			09	.....
ADDRESS REGISTER Rc2	0x0a-	02		05		08		0b		0e	11	.....
ADDRESS REGISTER Rc3	0x05-	01			04			07				.....
ADDRESS REGISTER RR		Rc1	Rc2	Rc3	Rc2	Rc1	Rc2	Rc3	Rc2	Rc1	Rc2	Rc3	.....
READ-OUT PIXEL DATA		(5,1)	(5,2)	(5,3)	(5,4)	(5,5)	(5,6)	(5,7)	(5,8)	(5,9)	(5,10)	(5,11)	.....

FIG. 16


SETTING PROCESS
S300
INITIALIZE UPDATE TIMING SIGNAL GENERATING UNIT AND SWITCHING CONTROL UNIT
S310
SET V_Rc1=INIT TO ADDRESS REGISTER Rc1 AND SET V_Ra1=+3 TO ADDITIONAL VALUE REGISTER Ra1
S320
SET V_Rc2=INIT+gap+2 TO ADDRESS REGISTER Rc2 AND SET V_Ra2=+3 TO ADDITIONAL VALUE REGISTER Ra2
S330
SET V_Rc3=INIT+1 TO ADDRESS REGISTER Rc3 AND SET V_Ra3=+3 TO ADDITIONAL VALUE REGISTER Ra3
END